All-Digital CDR for High-Density, High-Speed I/O

Matthew Loh, Azita Emami-Neyestanak
California Institute of Technology
1200 E California Blvd, M/C 136-93, Pasadena, CA 91125, USA, Tel: +1 (626) 395-2244, Email: rui@caltech.edu

Abstract

A novel all-digital CDR for source-synchronous links, and its implementation in 90nm CMOS, is presented. A phase alignment technique with ping-pong action between two clock phases is used. The system is implemented in static CMOS logic, occupies 0.234 mm^2 and dissipates 16.6 mW at 6 Gb/s, demonstrating BER $<10^{-13}$ with PRBS-7 input. The compactness and all-static-CMOS nature of the system make it suitable for use in high-speed I/Os requiring per-pin synchronization. (Keywords: CDR, static CMOS, all-digital)

Introduction

Most modern high-speed interconnect relies on both high data rates per pin and parallelism. Wide links tend to be source-synchronous; however, the delay between the clock and data paths can vary over time, making re-synchronization of the clock and data at the receiver necessary. As data rates increase, the mismatch between the data paths themselves has become large enough to require per-pin phase alignment [1]. Thus, a small, low-power CDR system is an important component of such interconnects.

This paper presents a novel all-digital CDR system for source-synchronous links (Fig. 1). By taking a digital approach, this design avoids the increasing size, power and complexity overheads faced by analog techniques in highly-scaled CMOS processes. Except for the front-end sense-amplifiers (StrongARM latches) the system is implemented entirely using static CMOS logic gates and the synchronization algorithm is synthesized from HDL into standard cells. Therefore, the design is highly portable and customizable, and its performance scales with the digital circuitry fed by the link. Finally, it collects data that can provide diagnostics for the link without extra hardware, useful for on-chip self-test and calibration.

Principle of Operation

The typical CDR uses a 2x oversampled data-clock/edge-clock technique and a PLL or a DLL. In this system, the edge clock is repurposed into a 'search-clock', not fixed at 90° relative to the data clock, but free to move within 2 unit-intervals (UI). This 2 UI delay is generated by an 'open' delay line that is slowly and digitally calibrated. The samples produced by the search-clock are compared with those produced by the data-clock, generating match/mismatch (M/MM) data. As the search-clock sweeps through 2 UI, the M/MM information is collected into a 'signature', which can be thought of as a binary reduction of an eye diagram (Fig. 2). By filtering the raw signature, the system can identify the middle of the eye, where the search-clock will be positioned to recover the data at the end of the sweep. *At this point the function of the search- and data- clocks is switched* and a new sweep cycle, with the old data-clock now acting as the search-clock, starts. This ping-pong action overcomes the key limitation of traditional delay-line-based systems; allowing the data phase to swap from one UI to an adjacent one between updates enables the realization of an infinite delay range. The 2 UI delay can be calibrated by ensuring that the distance between the end of one 'eye opening' and the end of the next is about half the available delay range.

In order to make M/MM decisions, the mismatch counter detects transitions in the incoming data and makes comparisons between the search and data samples when an appropriate transition occurs. Each phase position is observed for 32 transitions before a final M/MM decision is made. These decisions are then AND/OR filtered to prevent noise and transient events from corrupting the signature (Fig. 2).

Only two transitions from match to mismatch (marked 1 and 2 in Fig. 2) are required to detect the eye opening. In normal operation, signature collection is stopped after these are found to speed operation. A more complete search is only conducted when the data eye begins to drift off the extent of the delay line, or delay line calibration is required. For example, in Fig. 3 the phase offset between clock and data is gradually increasing. As data drifts to the right, the CDR tracks this shift and updates the data phase accordingly. However, when data drifts far enough, the edge of the current eye moves off the end of the delay line and cannot be found. The CDR then searches for M/MM transitions 3 & 4 to acquire the preceding eye opening. It places the updated data phase in this eye opening and trades the positive and negative edges of the clock, completing the UI swap.

The complete system was implemented in Matlab for performance characterization. The simulated sinusoidal jitter (SJ) tolerance using PRBS-31 input with 1ps RMS random jitter at 6 Gbps is shown in Fig. 5.

System Implementation

The delay line used to generate the 2 UI delay was implemented as a differential inverter chain with tri-state buffer calibration (Fig. 4) [2]. By turning tri-states on or off using signals en[7] to en[0], the drive strength of each stage can be changed, thus calibrating overall delay. Weak cross-coupled inverters are used to maintain phase alignment between the two paths. This scheme has the advantage of allowing the direct, digital modulation of delay in pure static CMOS. The output of the calibration stages is fed-forward, allowing a large delay range without using large tri-state buffers. Pre-buffer delay cells are used to equalize rise and fall times of the clock signal before the delay line core, to ensure the linearity of the output phases. The phase interpolator is a pair of inverters with shorted outputs.

In order to multiplex the top and bottom sample and clock paths into the data and search paths, the multiplexer must make its switch between the two clocks without adding or dropping a rising edge. Changes in the multiplexer control signal are delayed until both clocks are high, such that the two are swapped when no transition is occurring in either. Timing of this path is critical. If the delay line is properly calibrated, the two incoming clocks will be at most 90° out-of-phase; consequently, the switch must take place within a quarter of a clock period. To meet this timing requirement, the NAND gate (Fig. 4) output is rise time optimized.

Measurement Results

The system was implemented in 90 nm CMOS, occupying a core area of 550 µm x 425 µm. CDR functionality was

tested at 6 Gbps with PRBS-7 data, achieving a BER $<10^{-13}$. The CDR successfully corrects for an unlimited range of delay between the forwarded clock and the data. At 6 Gbps, net power consumption was 16.6 mW. A breakdown of performance is included in Table I. The clock-swapping multiplexer (Fig. 4) showed an unforeseen metastability problem, occasionally resulting in errors when swapping between the two clocks. This can be resolved by adding an extra flip-flop on the data_top input of the multiplexer.

As in most CDRs, phase generator linearity affects the overall performance of the system. DNL affects M/MM transition detection, measured to be 0.44 LSB. The data phase position is calculated as the average of two M/MM transitions and is affected by the INL, measured to be 1.6 LSB. Thus, overall error in the data phase position is 2.04 LSB (Fig. 7).

Conclusion and Acknowledgments

An all-static-CMOS implementation of a novel delay line-based CDR scheme for source-synchronous links has been presented. It is capable of realizing an infinite delay range and has low power consumption and small area characteristics.

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TABLE I
PERFORMANCE SUMMARY

Process	90nm CMOS
Die Area	1.75mm x 1.65mm
Core Area	550um x 425um
Data Rate	6Gbps
Supply Voltage/Power Dissipation	
Phase Generator, Latches	1.0V / 10.5mW
Control Logic	1.0V / 1.2 mW
Mux, Retiming, Mismatch Counter	1.2V / 4.9mW
Figures-of-Merit	
Power Dissipation	2.8 mW / Gbps
Area	0.039mm^2 / Gbps

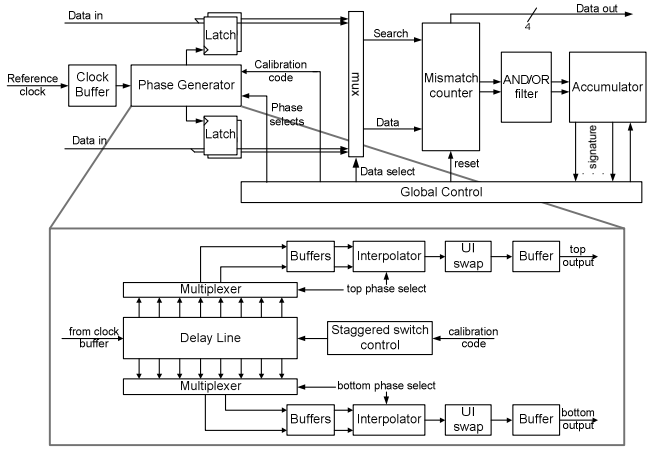

Fig. 1 Overall system architecture

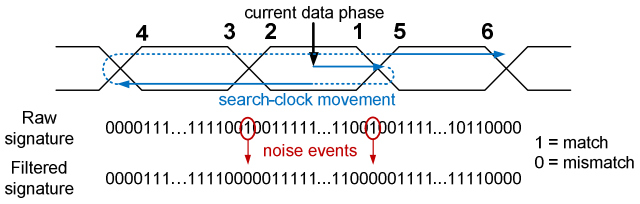

Fig. 2 M/MM transitions and raw/filtered signatures

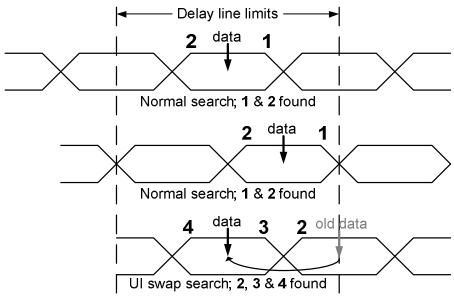

Fig. 3 CDR operation with data eye drifting until UI swap is required

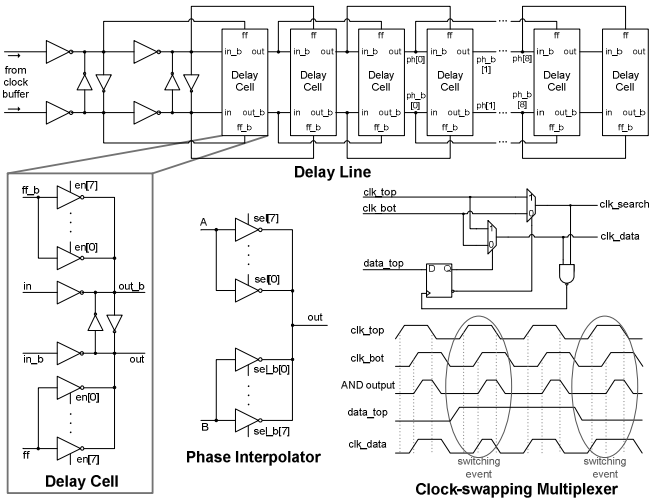

Fig. 4 Phase generator and multiplexer blocks

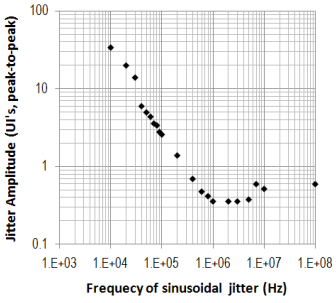

Fig. 5 Simulated SJ tolerance

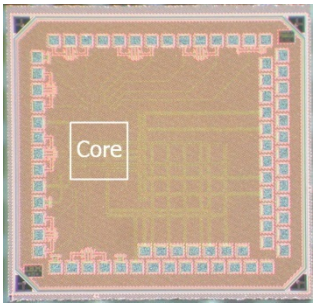

Fig. 6 Die micrograph

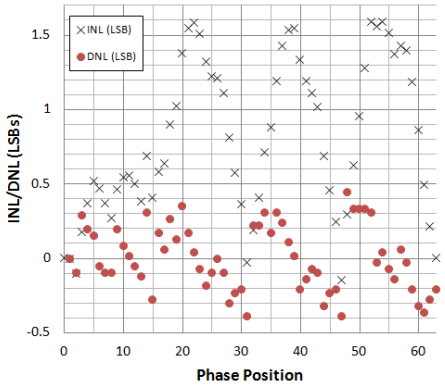

Fig. 7 Measured phase generator linearity

References

[1] N. Kurd et al, "Next generation Intel® micro-architecture (Nehalem) clocking architecture," IEEE Symposium on VLSI Ciruits, pp.62-63, June 2008

[2] J. Tierno et al, "A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI", IEEE J. Solid-State Circuits, vil. 43 pp. 42 – 51, Jan 2008